



11-29-02

2825

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: SAKIYAMA ET AL. Examiner: C. EVERHART
Serial No.: 09/700,940 Group Art Unit: 2825
Filed: NOVEMBER 21, 2000 Docket: 10873.589USWO
Confirmation No.: 4531
Due Date: NOVEMBER 29, 2002
Title: METHOD OF DISPOSING LSI

CERTIFICATE UNDER 37 CFR 1.10

'Express Mail' mailing label number: EV 043210338 US

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By: 

Name:

Commissioner for Patents
Washington, D.C. 20231

Sir:

We are transmitting herewith the attached:

- ☒ Transmittal Sheet in duplicate containing Certificate of Mailing
- ☒ Amendment Including Version With Markings To Show Changes Made
- ☒ Return postcard

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers or any future reply, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

MERCHANT & GOULD P.C.
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612.332.5300

By: 

Name: Douglas P. Mueller

Reg. No.: 30,300



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S/N 09/700,940

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AMENDMENT & RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In Response to the Office Action mailed on August 29, 2002, please consider and enter the following amendments and remarks.

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In The Claims

Please amend claims 1 and 4 as follows.

1. (Twice Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:

determining a capacitance value of the power supply capacitor cells so as to correspond to a drive load capacity value of the logic gate cells, and

arranging the power supply capacitor cells in a vicinity of the logic gate cells so as to connect a power supply line of the logic gate with a ground line of the logic gate through the power supply cells.

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